DesignWare 28-nm High-Speed Data Converter IP

**Highlights**
- Complete portfolio for analog interfaces in 28-nm includes high-speed ADCs and DACs, PLL, and general-purpose ADCs and DACs
- Standard CMOS process with no additional process options
- Parallel SAR 12-bit ADC architecture implementations for up to 320 MSPS sampling rates
  - Parallel assembly allows for greater architectural flexibility for specific applications
- Very high performance 12-bit 600 MSPS DAC
- Power consumption reduction of up to 3X and area use reduction of up to 6X over previous generations
- Reduced pin count and smaller external bill-of-materials (BOM) requirements

**Target applications**
- Cellular communications
- Wireless connectivity
- Multimedia, digital TV and radio reception (satellite, cable, terrestrial)
- Femto-cells and communications backhaul

**Technology Process**
- TSMC 28-nm HPM

**Overview**
Data converters are at the core of every analog interface to systems-on-chips (SoCs). As SoCs move into more advanced process nodes to benefit from process scaling, the challenge of integrating the analog interfaces becomes more serious due to the perceived bad analog characteristics of these processes, the reduced supply voltage available, and the large area requirements for these blocks. Synopsys' 28-nm DesignWare® Data Converter IP enables SoC designers to effectively move their designs into more advanced process nodes, and take advantage of the cost and power benefits that advanced nodes offer. These IP solutions are based on state-of-the-art architectures, including the Parallel Successive Approximation Register (SAR) architecture, which benefit from the characteristics of the advanced process nodes, while improving the overall analog IP performance and scaling down silicon area and power significantly.

Synopsys DesignWare 28-nm High-Speed Data Converter IP targets applications such as cellular and wireless connectivity as well as multimedia and digital TV. It includes 12-bit high-speed analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), 3 GHz low jitter PLLs, and 12-bit general-purpose ADCs and DACs. The IP features very small area and power consumption, making it the solution of choice for designers who need to meet challenging cost and power targets.

Synopsys’ high-quality DesignWare Data Converter IP solutions have been implemented in more than 200 production designs, giving designers confidence that they can successfully integrate high-performance analog IP into their SoCs with less risk and improved time-to-results.
Complete Portfolio

- 12-bit 80 MSPS ADC and IQ-ADC
- 12-bit 320 MSPS ADC and IQ-ADC
- 12-bit 600 MSPS DAC and IQ-DAC
- 12-bit 5 MSPS General-Purpose SAR ADC with 8:1 analog input multiplexer
- 12-bit 20 MSPS General-Purpose DAC with single ended voltage output
- Low jitter 3 GHz PLL for sampling clock generation

Receive ADC

The DesignWare ADC is based on the 12-bit Parallel SAR architecture. SAR-based architectures can take full advantage of the speed and processing power of advanced nodes to drastically reduce power and area.

To avoid the shortfalls of advanced nodes and guarantee the robustness of the ADC’s dynamic range and accuracy parameters, the ADC makes extensive use of digital compensation and calibration techniques. These techniques also reduce area and power by as much as 6x (area) and 3x (power) when compared to ADCs available in previous nodes.

The solutions for the receive ADC range from a 12-bit 80 MSPS ADC up to a 12-bit 320 MSPS ADC, both in single and dual (IQ) channel configuration, giving designers full IP flexibility to match their specific requirements.

12-bit up to 320 MSPS ADC Features

- 12-bit Resolution SAR-based ADC
- 12-bit Resolution SAR-based IQ-ADC
- Matched dual channel configuration
- Low clock speed requirement: up to 320 MHz
- Low latency
- Support 1Vppdiff input signal
- Compact area
- Low power consumption
- Reduced BOM
  - No external components for reference
  - Small pin count
- Robust for deep sub-micron nodes
  - Amplifier-less architecture
  - Digital calibration of capacitor array and comparator offset
- Core supply operation

Transmit DAC

The 12-bit 600 MSPS high performance DAC implements a traditional current steering architecture with advanced digital techniques to improve dynamic performance and linearity at very high signal frequencies, thus enabling users to effectively use higher oversampling rates and other IF techniques to simplify their system and save power. These techniques have the additional benefit of reducing area and power by as much as 3x when compared to previous generations.

The solutions for the transmit DAC include both single and dual (IQ) channel configurations. It is equally effective for low and high sampling rate applications.

12-bit IQ-DAC up to 600 MSPS Features

- 12-bit Resolution Current Steering DAC
- 12-bit Resolution Current Steering IQ-DAC
  - Matched dual channel configuration
  - Core supply operation
  - Up to 600 MSPS
- Programmable full scale current
  - 1 to 5mA full-scale range

Figure 1: Baseband Analog Interface block diagram
500mV compliance range
Small area
Reduced BOM and pin count
High performance for large bandwidth (BW) signals
Digital noise reduction (DWA)

Clock-generating PLL
The Synopsys analog interface solution includes a companion PLL to generate the sampling clock signal to the data converters. This compact and low-power analog PLL employs a robust architecture that enables the generation of a low-jitter clock with high flexibility, making it suitable as a clock generator for systems processing broad and narrow band signals.

Clock-generating 3GHz PLL Features
- Ring oscillator VCO up to 3 GHz
- Minimum input frequency 20 MHz
- Flexible clock generation
- Very compact and low power consumption
- Fast lock mode
- Programmable clock multiplication rate
- Low jitter: meets the jitter requirements for all required protocols

General-purpose ADC and DAC Features
- 12-bit 5 MSPS SAR ADC with 8:1 analog input multiplexer for general-purpose measurements
- Internal reference generation
- 12/10/8 and 6-bit resolution modes
- 12-bit 20 MSPS DAC with output voltage buffer for closed loop control
- Low noise
- Current mode output
- Compact and low power

Additional Analog IP Portfolio available in 28-nm
- 10-bit 300 MSPS triple Video DAC (VDAC)
- 96-dB Analog Audio Codec

Deliverables
- Databook
- Behavioral Verilog model
- Abstract LEF and timing LIB files
- CDL netlist for LVS
- GDSII layout database
- Assembly guidelines and full integration support

About DesignWare IP
Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes complete interface IP solutions consisting of controllers, PHY and verification IP for widely used protocols, analog IP, embedded memories, logic libraries, processor cores and subsystems. To support software development and hardware-software integration of the IP, Synopsys offers drivers, transaction-level models, and prototypes for many of its IP products. Synopsys' HAPS® FPGA-Based Prototyping Solution enables validation of the IP and the SoC in the system context. Synopsys' Virtualizer™ virtual prototyping tool set allows developers to start the development of software for the IP or the entire SoC significantly earlier than traditional methods. With a robust IP development methodology, extensive investment in quality, comprehensive technical support, software development and IP prototyping support, Synopsys enables designers to accelerate time-to-market and reduce integration risk.

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